PETsys Electronics
Medical PET Detectors S.A.

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PETsys Electronics

PETsys SiPM Readout System

§ 1. Introduction.

The PETsys SiPM readout system is designed for applications requiring the readout of large numbers of SiPM channels with high data throughput and excellent timing resolution. The system was originally developed for Time-of-Flight PET applications, but it is equally suitable for many other applications requiring the readout of large numbers of SiPM channels. The system is typically equipped with PETsys TOFPET2-C ASICs, but can also be equipped with PETsys TOFPET 2D ASICs. The TOFPET 2D version can process either positive or negative input pulses, allowing the system to interface directly with Micro-Channel Plate PMTs and other sensors producing negative signals.

The readout system is based on the PETsys TOFPET2 ASIC [1], a low-power 64-channel ASIC optimized for SiPM readout in TOF-PET applications. See our website under "Downloads" for the data sheet of the ASIC. The ASIC interfaces directly with the photosensors and digitizes the detected events. Whenever the signal in a channel exceeds the configurable thresholds, an event record containing channel number, timestamp and charge information is generated. Beyond the ASIC, the complete readout chain is fully digital.

The readout system consists of four main components: the Front-End Modules, the Front-End type-D units, the Clock & Trigger unit, and the DAQ unit. Together these modules form a scalable data-acquisition platform capable of reading tens of thousands of independent SiPM channels.

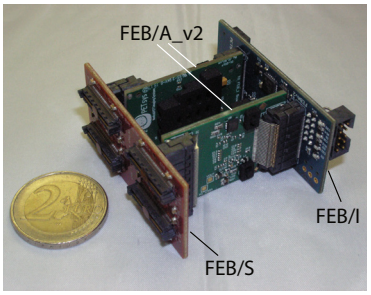

Figure 1. The FEM128 module incorporates two TOFPET2 ASICs and provides 128 SiPM readout channels.

§ 2. The PETsys Front-End modules.

The PETsys Front-End Modules (FEM) provide the interface between the analog sensor signals and the fully digital readout chain. Different Front-End Modules are available and can be adapted to specific detector geometries and SiPM arrays. Two standard versions are currently available: FEM128 and FEM256.

The FEM128 module (Fig. 1) provides 128 readout channels and is optimized for applications requiring high per-channel event rates. The FEM128 is made up of three different boards: FEB/A, FEB/S and FEB/I. The FEM128 has two FEB/A boards (Fig. 2). Each FEB/A board has one PETsys TOFPET2 ASIC with 64 channels. The FEB/A boards are mounted perpendicular to the SiPM arrays, simplifying thermal stabilization and detector cooling. The board also has a temperature sensor near the ASIC.

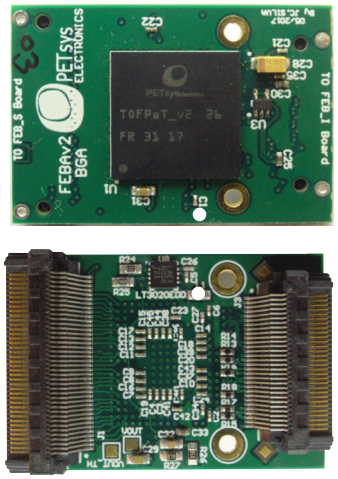

Figure 2: Top and bottom views of the FEB/A_v2 board.

The FEB/S board is a passive adapter board matching the selected SiPM array to the FEB/A input connectors. Different FEB/S versions are available for different SiPM arrays. The version shown in Figure 1 directly supports Hamamatsu MPPC arrays S13361-3050AS-08, S13361-3075AE-08. The FEB/S board is four-side buttable, allowing the construction of detector planes with minimal dead space.We can supply the FEM128 with a FEB/s taking the ONSemi ARRAYJ-300XX-64P-PCB SiPM array instead of the Hamamatsu SiPM array, and we have a number of non-standard FEB/S for several other SiPM arrays.

The FEB/I board interfaces the FEM128 to the FEB/D units. It incorporates a MAX10 FPGA, converts the communication protocol between LVCMOS and LVDS, and digitizes the analog temperature sensor signals. Up to eight FEM128 modules can be connected to one FEB/D-1k unit using a SAMTEC HQDC-030-xx.00- TTL-SBL-1N flat coax cable (Fig. 3). This cable can be up to 3 m long. Depending on cable length, an auxiliary Molex power cable may be required.

Figure 3: SAMTEC HQDC flat coax cable used to connect FEM modules to the FEB/D unit.

Using the recommended operating settings, the ASIC power dissipation is approximately 8.6 mW/channel. Lower-power operating modes down to 4 mW/channel are also available, with a modest reduction in timing performance. Including LVDS buffers and local voltage regulators, the total FEM128 power consumption is approximately 1.9 W.

[1] Experimental characterization of the TOPET2 ASIC, R. Bugalho et al. JINST **14** P0329

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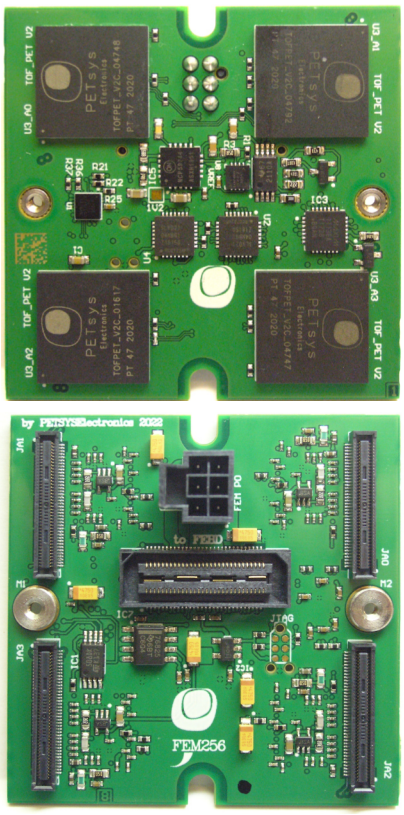

Figure 4. Top and bottom side of the PETsys FEM/256 board.

Figure 5. Example of a detector module built around the FEM256 board. The cooling solution must be adapted to the specific scanner geometry.

In the FEM128, each ASIC outputs data over four LVDS lines operating at 800 Mbps per line. Events are encoded in 80-bit records. The maximum event rate between the FEM128 module and the FEB/D-1k unit is approximately 500 kcps per channel. However, the FEB/D-8k can only acquire data at 400 Mbps per data line, reducing the maximum event rate to approximately 300 kcps per channel.

The FEM256 module is optimized for large systems and reduced cost per channel. It enables more compact detector modules and simplifies the design of the cooling system.

The FEM256 board is shown in Figure 4. In this front-end board, the functionality of the FEB/A and FEB/I boards used in the FEM128 architecture is combined into a single board. The FEM256 incorporates a MAX10 Altera FPGA, which converts the communication protocol from the LVCMOS interface used by the FEB/D unit to the LVDS interface required by the ASICs, and reads the analog temperature sensors. The board measures 50 × 50 mm² and connects to the FEB/D unit using the same SAMTEC HQCD cable shown in Figure 3.

In the FEM256 architecture, each ASIC uses two LVDS data lines for data output. As a result, the maximum event rate is limited to approximately 300 kcps per channel when connected to a FEB/D-1k, unit and to 150 kcps per channel when connected to a FEB/D-8k. Up to four FEM256 modules can be connected to a FEB/D-1k unit, while up to sixteen modules can be connected to a FEB/D-8k unit.

Figure 5 illustrates a possible integration of the FEM256 with the detector mechanics and cooling system. An aluminum cooling bar is inserted between the FEM256 board (top) and the FEB/S-256 board (bottom), which carries the SiPM arrays. The SiPM arrays may either be reflow-soldered directly onto the FEB/S-256 board or mounted on a FEB/S version equipped with connectors. The ASICs on the FEM256 are in direct thermal contact with the cooling bar. In addition to providing efficient heat removal, the cooling bar also serves as a mechanical reference for positioning the SiPM arrays.

The FEB/S-256 board measures 52 × 52 mm². Flexible cables route the signals from the SiPM arrays to the ASICs. Figure 5 is intended to illustrate the integration concept only; the mechanical implementation of the front-end module must be adapted to the specific requirements of each scanner design.

Comparison FEM128 FEM256	FEM128	FEM256
Number of ASICs	2	4
Number of Channels	128	256
Number of Temperature sensors	2+2	4+4
Number of LVDS data output Links per ASIC	4	2

§ 3. The PETsys Front-End type-D unit.

The PETsys Front-End Type D (FEB/D) unit collects event records from the ASICs and transmits them to the data acquisition (DAQ) computer as assembled data frames. Two versions of the FEB/D unit are available. The FEB/D-1k is optimized for small and medium-sized systems with up to 16,384 channels, while the FEB/D-8k is designed for larger systems requiring higher channel counts and increased data throughput.

Multiple FEB/D units can be operated synchronously through a connection to the Clock & Trigger unit using an ERNI SMC connector carrying LVDS signals at 400 Mbit/s. In addition to distributing the system clock and synchronization signals, this interface supports a hardware trigger system that can reject event records that are not part of a coincidence. Such events are discarded before transmission to the DAQ computer, reducing data bandwidth requirements. The FEB/D unit can also receive external veto signals from the Clock & Trigger unit.

The FEB/D units provide clock and synchronization signals to the ASICs and receive configuration signals from the DAQ unit and distribute these to the ASICs. Each FEB/D unit receives the system clock (200 MHz), and synchronization and trigger signals from the Clock & Trigger unit.

All FEB/D units are equipped with a communication mezzanine. Three communication options are available.

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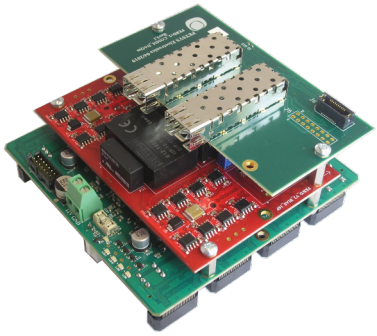

Figure 6: Top view of the FEB/D-1k unit showing the bias voltage mezzanine (red) and the SFP+ communication mezzanine (green) on top of it.

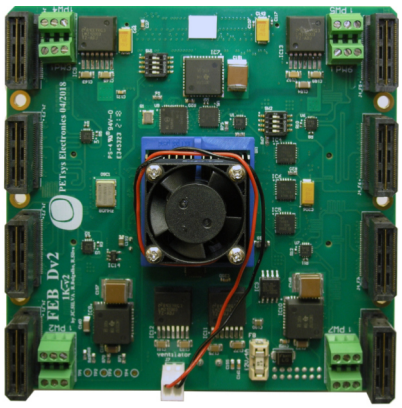

Figure 7. Bottom view of the FEB/D-1k motherboard showing the 8 connectors receiving the cables from the FEM128 modules

The Gigabit Ethernet mezzanine is intended for small systems. In this configuration, the maximum sustained data output rate to the DAQ computer is approximately 15 million events per second.

The SFP+ communication mezzanine provides two SFP+ ports. One port is used for data transmission and configuration, while the second port allows multiple FEB/D units to be daisy-chained. The ports support either optical transceivers or direct-attach copper cables. Up to 32 FEB/D-1k units can be connected in a single chain. Operating at 6.6 Gbit/s, the SFP+ interface supports an aggregate data throughput of up to 100 Mcps per second per chain.

The QSFP+ communication mezzanine provides a higher-bandwidth optical interface and supports data rates of up to 200 Mcps to the DAQ computer.

The FEB/D-1k unit

The FEB/D-1k unit is shown in Figures 6 and 7. It consists of a motherboard equipped with a Xilinx Kintex-7 XC7K160T FPGA, a communication mezzanine, and a bias-voltage mezzanine. The motherboard measures 104.5 × 104.5 mm². On-board DC-DC converters and voltage regulators generate the low-voltage supplies required by the ASICs located on the FEM modules.

A single FEB/D-1k unit can interface with up to eight FEM128 modules. Depending on the power configuration, it can also support up to four FEM256 modules when the ASIC power is supplied by the FEB/D motherboard, or up to eight FEM256 modules when the ASIC power is supplied by external power supplies.

The middle mezzanine (the red board in Figure 6) supplies bias voltages to the SiPMs. The bias-voltage mezzanine generates the bias voltages required by the SiPM arrays. The standard version provides 16 independently programmable positive bias voltages in the range of 0-72 V, with a maximum output current of 2.5 mA per channel. A version providing up to 8.75 mA per channel is also available. The SiPM bias voltages can be supplied by an external power supply.

When connecting a FEM128 or FEM256 to the FEB/D-1k, use a Samtec cable no longer than than 50 cm for a FEM128, or no longer then 25 cm for a FEM256. Longer Samtec cables require an additional power cable.

Main features of the FEB/D-1k unit:

- Equipped with Kintex-7 (XC7K160T) FPGA with pre-installed firmware.
- Supports up to eight FEM128 modules.
- Supports up to four FEM256
- Maximum output rate to DAQ of 100 Mcps/s when using SFP+ comm. mezzanine and 200 Mcps/s when using QSFP+ communication mezzanine.
- Up to 32 FEB/D-1k units can be daisy-chained and connected to a single DAQ unit input.
- Clock frequency 200 MHz.
- External supply voltage: 12 Vdc, maximum 4 A.
- On-board DC-DC converters supply power to the ASICs in the FEM boards.
- Programmable SiPM bias voltages generated on a dedicated mezzanine board.The default mezzanine provides 16 lines, 5-75 V, positive, 2.5(standard) -8.75(optional) mA per bias line.

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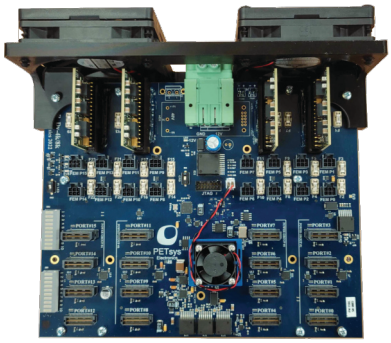

Figure 8. Top view of the FEB/D-8k motherboard

The FEB/D-8k unit

The FEB/D-8k is designed for large-scale PET systems and can interface with up to 16 front-end modules, either FEM128 or FEM256.

The FEB/D-8k is equipped with both a Xilinx Kintex-7 XC7K160T FPGA and a Spartan-7 XC7S50 FPGA. As shown in Figures 8 and 9, the unit consists of a motherboard measuring 208 × 166.3 mm² and three mezzanine boards mounted on its underside. The green mezzanine provides the communication interface, while the two red mezzanines generate the SiPM bias voltages.

The standard bias-voltage configuration provides 32 independently programmable positive bias voltages in the range of 0–60 V, with an average output current of 2 mA per channel. A 5 mA version is available on request.

The FEB/D-8k operates from a 12 VDC power supply and can draw up to 25 A, depending on the system configuration. Four on-board DC-DC converters provide the low-voltage supplies required by the ASICs located on the front-end modules. The standard configuration uses Texas Instruments DC-DC converters.

Front-end modules are connected to the FEB/D-8k using SAMTEC HQCD cables. The maximum cable length depends on the system configuration. The table below summarizes allowable HQCD cable length for FEB/D-8k. For longer cables an additional Molex cable is required. The maximum supported HQCD cable length is 3 m. Further details are provided in the user manual.

The current version of the FEB/D-8k supports data reception from the ASICs at 300 kcps per channel for FEM128 modules and 150 kcps per channel for FEM256 modules.

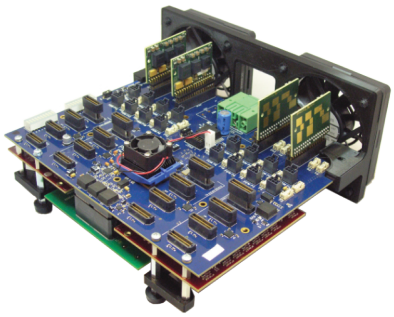

Figure 9. On the top side of the FEB/D-8k motherboard there are four 4 DC-DC converters providing power to the ASICs and 16 connectors for the FEM modules. Under the motherboard there are two bias mezzanines and one communication mezzanine

Allowable HQCD cable length for FEB/D-8k	
DC-DC type	Texas Instruments
FEM128	100 cm
FEM256	50 cm

Main features of the FEB/D-8k unit :

- Reads up to 4’096 independent SiPM channels from 16 FEM modules.
- Equipped Kintex-7 XT7K160T and Spartan 7 XC7S50 FPGA with pre-installed firmware.
- Connects to up to 16 Front-End Modules either FEM128 or FEM256.
- Max output rate to DAQ of 100 Mcps/s when using SFP+ communication mezzanine and 200 Mcps/s when using QSFP+ comm mezzanine
- Up to 32 FEB/D-8k units can be daisy-chained and connected to a single DAQ unit input.
- Clock frequency 200 MHz.
- External supply voltage: 12 Vdc, 25 A.
- On-board DC-DC converters supply power to the ASICs in the FEM boards.
- SiPM bias voltages produced by two mezzanine boards. The default mezzanine type provides 32 biasing lines, independently configurable to 0-60 V, and able to supply 2 mA per bias line on average.

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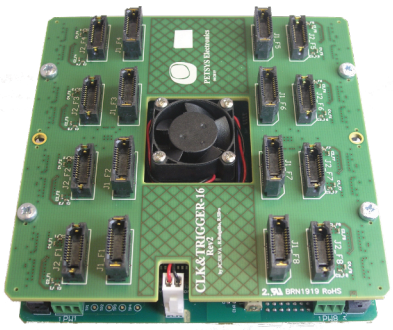

Figure 10: Bottom view of the Clock & Trigger unit showing the connectors for 16 Samtec ERCD cables providing Clock & Trigger signals to the FEB/D units.

4. The Clock & Trigger Unit

The Clock & Trigger unit (see Figure 10) provides the timing backbone of the PETsys readout system. It distributes the system clock and synchronization signals to all FEB/D units and ensures that all detector modules operate as a single synchronized system.

In addition to clock distribution, the unit can perform real-time coincidence selection. It receives coarse timing information from all FEB/D units and identifies which events belong to valid coincidences. Event-selection decisions are then returned to the FEB/D units, allowing unwanted events to be rejected before they are transmitted to the DAQ computer. This significantly reduces the required data bandwidth for large systems.

The Clock & Trigger unit uses the same motherboard, communication mezzanine, and communication protocol as the FEB/D units. It can be connected in the same communication chain as the FEB/D units and requires no dedicated DAQ interface. It has two versions, namely the Clock & Trigger-16 and the Clock&Trigger-64.

A single Clock & Trigger-16 unit supports up to 16 FEB/D units and up to four trigger regions per FEB/D.The Clock & Trigger-64 unit supports up to 64 FEB/D units and one trigger region per FEB/D.

For integration with external equipment, the unit can either accept or generate clock and synchronization signals. It can also receive an external veto signal, allowing data acquisition to be temporarily inhibited across the entire detector system.

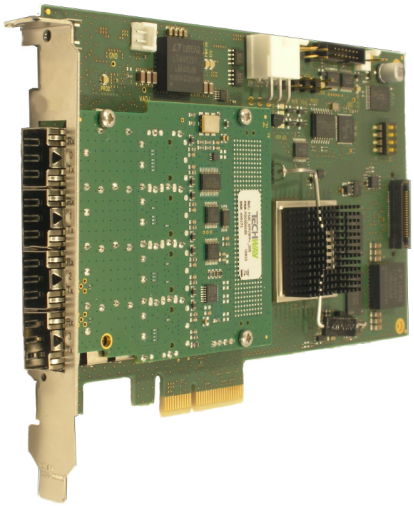

Figure 11: Standard version of the DAQ4 unit with four SFP+ connectors on the front panel .

5. The DAQ4 Data Acquisition Interface

The DAQ4 unit is the interface between the PETsys readout electronics and the data acquisition computer. Installed directly in a PCI Express slot, it receives event data from the FEB/D units and transfers the data to the host computer for storage and processing.

Besides data transfer, the DAQ4 is responsible for configuring the complete readout system. It distributes ASIC configuration data, monitors detector temperatures, reads diagnostic information from the electronics, and controls the Clock & Trigger unit.

The standard DAQ4 version is equipped with four SFP+ communication ports, each supporting optical transceivers or direct-attach copper cables. Every SFP+ link can receive up to 100 million events per second from a chain of FEB/D units.

For applications requiring higher throughput, the DAQ4 can alternatively be equipped with two QSFP+ ports. In this configuration, each QSFP+ link supports up to 200 million events per second.

Main features of the DAQ4 unit.

- PCI Express data-acquisition card for PETsys TOFPET2-based systems.
- Equipped with Kintex 7 (XC7K325T) FPGA with pre-installed firmware.
- Compatible with FEM128, FEM256, FEB/D-1k, FEB/D-8k and Clock & Trigger
- The DAQ4 has 4 PCI Express Gen 2 lanes
- Available with either four SFP+ ports or two QSFP+ ports
- Maximum 100 M events/s for each SFP+ input
- Maximum 200 M events/s for each QSFP+ input
- Maximum data output rate to the DAQ computer: 230 M events/s.
- Reads front-end temperature sensors..
- Reads diagnostic and monitoring information from the TOFPET2 ASICs.

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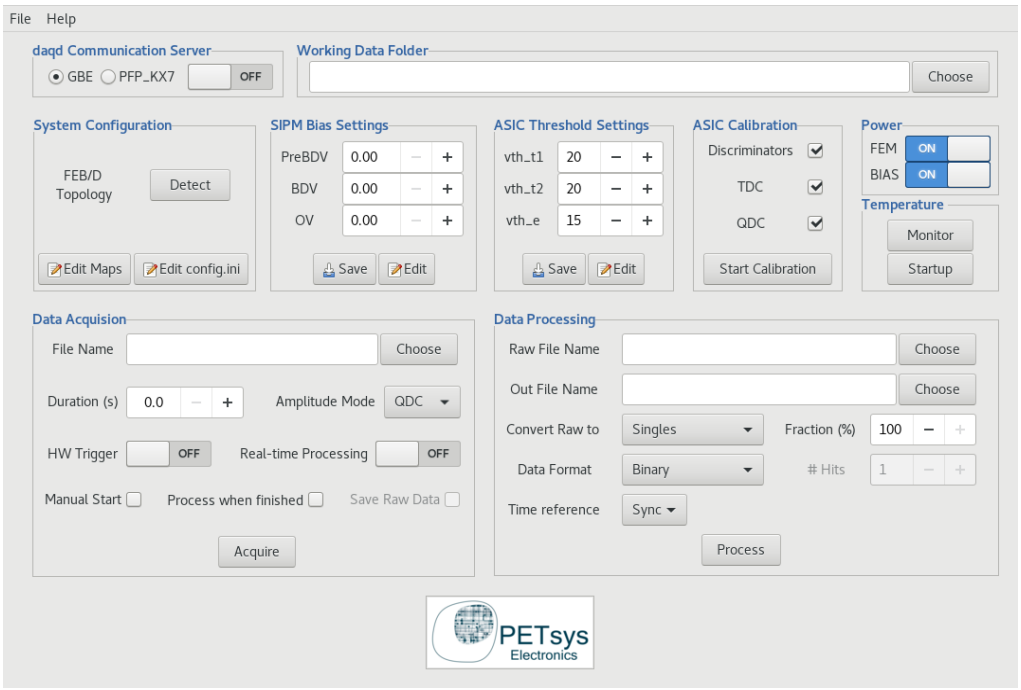

Figure 12: The data-acquisition is controlled by an easy-to use graphical user interface.

6. Data Acquisition Firmware and Software

The PETsys readout system is supplied with both firmware and data-acquisition software. The software is supported on Alma Linux 8 or later, Red Hat Enterprise Linux 8.5 or later, and Ubuntu 20.04 or later.

The system includes an intuitive and easy-to-use graphical user interface (Figure 12) for detector configuration, calibration, monitoring, and data-acquisition. For advanced users, the complete data-acquisition software source code is provided under the MIT open-source license. This software is written in Python and C++ and enables full customization and integration into existing research frameworks.

The software and firmware have been designed to provide direct access to the detector electronics while preserving maximum flexibility for the user. Configuration parameters, bias voltages, temperature measurements, calibration settings, and raw event data can all be accessed online during operation. Unlike many commercial PET acquisition systems, the PETsys readout chain performs minimal processing on the acquired data. Event records generated by the TOFPET2 ASICs are transferred to the DAQ computer essentially unchanged, giving users complete control over calibration and event selection.

To increase the effective data-acquisition rate, the firmware can discard uninteresting events in the FEB/D units, before the data reaches the DAQ computer. Each FEB/D can be divided into up to 4 readout regions. These readout regions can be grouped into user defined trigger regions. The coincidence filter only accepts events that have a matching partner in another trigger region within the coincidence window. This user defined coincidence window is based on timestamps with a resolution of 5 ns. Additional selection criteria can be applied using the total deposited energy within a trigger region or the coincidence multiplicity. All filtering parameters are fully configurable and can be optimized to match the geometry and operating conditions of a specific detector system.

Support for Random-Coincidence Correction

The firmware provides several options that facilitate the measurement and correction of random coincidences. Extended coincidence windows may be used to intentionally collect larger numbers of random events, providing functionality similar to the delayed-window method commonly used in PET.

In addition, the firmware can periodically acquire unbiased samples of single-event data. These samples can be used to estimate random-coincidence rates and to validate reconstruction algorithms without significantly increasing the overall data volume.

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Synchronization with other systems

Many applications require synchronization between the PET detector and external equipment such as MRI systems, beam instrumentation, motion-tracking systems, or external trigger electronics.

The PETsys architecture supports several synchronization methods. A common clock and synchronization signal can be shared between the PET readout system and external equipment whenever the clock frequencies are compatible. External timing signals may be connected directly to the FEB/D or Clock & Trigger units, where they are converted into timestamped event records with a timing granularity of approximately 1.25 ns.

For applications requiring the highest timing precision, external timing signals can also be connected directly to TOFPET2 input channels, allowing timestamps to be generated with the full timing precision of the ASIC.

The Clock & Trigger unit can additionally generate programmable LVDS timing outputs synchronized to the system clock, allowing the PET readout system itself to serve as the timing reference for other equipment.

7. Example readout configurations.

The PETsys readout architecture is highly scalable. By combining Front-End Modules (FEM), FEB/D units, Clock & Trigger units, and DAQ4 interfaces to the data acquisition computer, systems can be configured for applications ranging from small laboratory prototypes to large total-body PET scanners.

The examples below illustrate three typical system configurations.

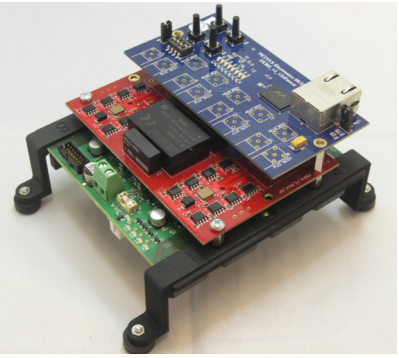

Figure 13. FEB/D-1k unit equipped with the Ethernet communication mezzanine for small systems.

Compact Readout Solution for Small Systems

Small detector prototypes and laboratory test setups often require only a few hundred to one thousand readout channels. In these applications, simplicity and low system cost are usually more important than maximum data throughput.

For systems with up to 1024 channels and a data rate below approximately 15 million events per second after coincidence filtering, a single FEB/D-1k unit equipped with a Gigabit Ethernet communication mezzanine is sufficient (Figure 13).

The FEB/D-1k directly interfaces with up to eight FEM128 modules and communicates with the data acquisition computer through a standard Gigabit Ethernet connection. No Clock & Trigger unit or DAQ4 interface is required. Typical applications include:

- Detector development and characterization
- Laboratory test benches
- Small animal PET prototypes
- Educational and research systems

Readout Solution for Medium-Size Systems

Applications requiring several thousand channels, or higher event rates, need the full PETsys architecture, including a Clock & Trigger unit and a DAQ4 interface to the data acquisition computer.

Figure 14 illustrates a typical system with 6'144 channels. The system consists of:

- 48 FEM128 modules
- 6 FEB/D-1k units
- 1 Clock & Trigger unit
- 1 DAQ4 interface

The FEB/D units are connected to the DAQ4 in a daisy chain using SFP+ links, while the DAQ4 communicates with the acquisition computer through a PCI Express interface. The Clock & Trigger unit distributes clock, synchronization, trigger and veto signals throughout the system.

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- This architecture is suitable for:
- Preclinical PET scanners
- Organ-specific PET systems
- PET detector demonstrators
- Non-destructive testing and industrial imaging systems
- Angular Correlation of positron Annihilation Radiation (ACPAR)
- Muon-detection-based imaging systems

Without firmware filtering, the event transfer rate between the DAQ4 and the host computer becomes the limiting factor and limits the event rate to ≈38 kcps per channel.

The effective acquisition rate strongly depends on the efficiency of the firmware filtering. Depending on detector geometry and operating conditions, the firmware filter increases the useful event throughput by a factor typically between two and ten.

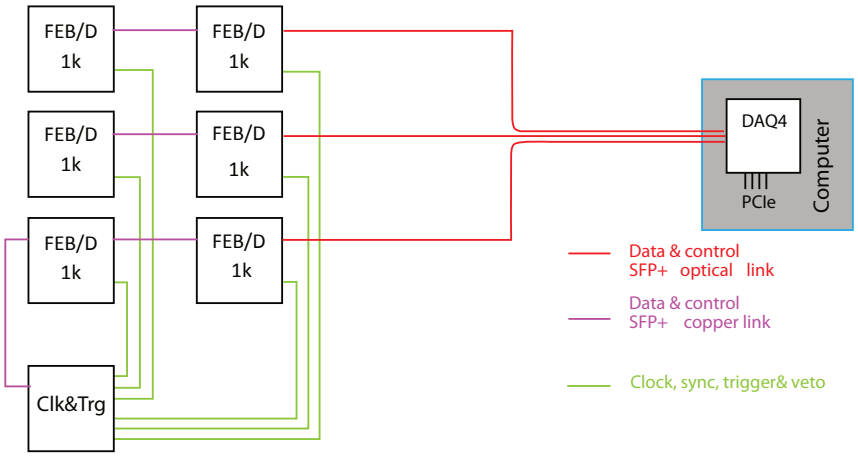

Figure 14. System interconnect topology for a system reading 6'144 channels.

Readout Solution for large systems

Large systems such as whole-body PET scanners require tens of thousands of readout channels while maintaining a low cost per channel.

Figure 15 shows an example system with 65'536 channels. The configuration consists of:

- 256 FEM256 modules
- 16 FEB/D-8k units
- 1 Clock & Trigger unit
- 2 DAQ4 interfaces

Each FEB/D-8k unit reads 16 FEM256 modules and directly transmits event data to one of the DAQ4 interfaces using high-speed SFP+ optical links.

Typical applications include:

- Whole-body PET scanners
- Total-body PET systems
- High-channel-count research instruments
- Large-area detector arrays

Also in this case, without firmware filtering, the data transfer rate between the DAQ4 and the host computer becomes the limiting factor and limits the event rate to ≈7 kcps per channel.

As with medium-size systems, the effective acquisition rate strongly depends on the efficiency of the firmware filtering. Depending on detector geometry and operating conditions, the firmware filter increases the useful event throughput by a factor typically between two and ten.

Large systems also require an acquisition computer with a motherboard supporting multi-GPU (two PCIe slots that are directly connected to the CPU), and equipped with multi-core high-performance CPUs and high-speed NVMe SSD storage.

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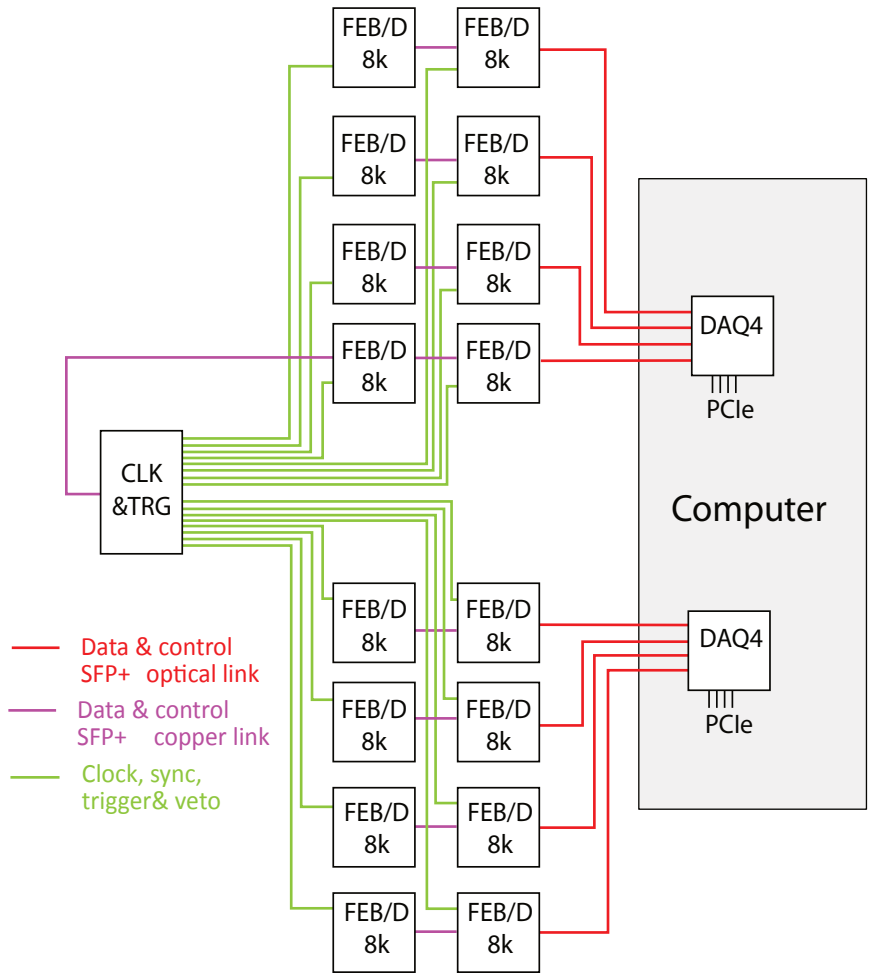
Figure 15. System interconnect topology for a system reading 65’536 channels.



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